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PTO/SB/05 (12/97)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new non-provisional applications under 37 CFR 1.53(b)

Attorney Docket No. 042390.P9737 Total Pages 2

First Named Inventor or Application Identifier Tony Hamilton

Express Mail Label No. EL627466588US

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 18)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 2)

4. X Oath or Declaration (Total Pages 5)

a. ___ Newly Executed (Original or Copy)

b. ___ Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**

i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. __ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. __ Microfiche Computer Program (Appendix)

7. __ Nucleotide and/or Amino Acid Sequence Submission

(if applicable, all necessary)

a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. _____ Assignment Papers (cover sheet & documents(s))
9. _____ a. 37 CFR 3.73(b) Statement (where there is an assignee)
_X_ b. Power of Attorney
10. _____ English Translation Document (if applicable)
11. _____ a. Information Disclosure Statement (IDS)/PTO-1449
_____ b. Copies of IDS Citations
12. _____ Preliminary Amendment
13. _X_ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. _____ a. Small Entity Statement(s)
_____ b. Statement filed in prior application, Status still proper and desired
15. _____ Certified Copy of Priority Document(s) (if foreign priority is claimed)

16. Other: Certificate of Express Mail with copy of postcard showing contents of Express Mail package.

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:

___ Continuation ____ Divisional ____ Continuation-in-part (CIP)

of prior application No: _____

18. **Correspondence Address**

_____ Customer Number or Bar Code Label _____
(Insert Customer No. or Attach Bar Code Label here)

or

_X_ Correspondence Address Below

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FEE TRANSMITTAL FOR FY 2000

TOTAL AMOUNT OF PAYMENT ($) $1296.00

Complete if Known:

Application No.	Not Yet Assigned
Filing Date	Herewith
First Named Inventor	Tony Hamilton
Group Art Unit	Not Yet Assigned
Examiner Name	Not Yet Assigned
Attorney Docket No.	042390.P9737

METHOD OF PAYMENT (check one)

1. [X] **The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:**

   Deposit Account Number 02-2666
   Deposit Account Name _____

   [X] **Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17**

---

2. X **Payment Enclosed:**
   X **Check**
   _____ **Money Order**
   _____ **Other**

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	690	201	345	Utility application filing fee	690.00
106	310	206	155	Design application filing fee	
107	480	207	240	Plant filing fee	
108	690	208	345	Reissue filing fee	
114	150	214	75	Provisional application filing fee	

SUBTOTAL (1) $ 690.00

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims	45	– 20** =	25	X	18	=	450.00
Independent Claims	5	– 3** =	2	X	78	=	156.00
Multiple Dependent						=	

****Or number previously paid, if greater; For Reissues, see below.**

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	260	204	130	Multiple dependent claim, if not paid
109	78	209	39	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) $ 606.00

Patent fees are subject to annual revisions. Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid.
See Forms PTO/SB/09-12

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for response within first month	
116	380	216	190	Extension for response within second month	
117	870	217	435	Extension for response within third month	
118	1,360	218	680	Extension for response within fourth month	
128	1,850	228	925	Extension for response within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing a brief in support of an appeal	
121	260	221	130	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive unavoidably abandoned application	
141	1,210	241	605	Petition to revive unintentionally abandoned application	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	690	246	345	For filing a submission after final rejection (see 37 CFR 1.129(a))	
149	690	249	345	For each additional invention to be examined (see 37 CFR 1.129(a))	

Other fee (specify) _____

Other fee (specify) _____

SUBTOTAL (3) $ 0

*Reduced by Basic Filing Fee Paid

SUBMITTED BY:

Typed or Printed Name: John Patrick Ward, Esq.

Signature _____ Date September 30, 2000

Reg. Number 40,216 Deposit Account User ID _____ (complete if applicable)

Attorney Docket: 42390.P9737 *PATENT*

UNITED STATES PATENT APPLICATION

FOR

METHOD AND APPARATUS FOR PROVIDING DYNAMICAL SCALABILITY

INVENTORS:

TONY HAMILTON

METHOD AND APPARATUS FOR PROVIDING DYNAMICAL SCALABILTY

FIELD OF THE INVENTION

This invention relates to computers. Specifically, this invention relates to providing dynamical scalability to portable computers, including notebook computers.

BACKGROUND OF THE INVENTION

Portable systems, such as notebook computers, have steadily become more powerful with improved technology. Notebook computers are popular because they are mobile and can be used in remote places such as on airplanes. They can also be used in homes and offices with accesses to AC outlets.

As the processor and bus speeds steadily rise and the graphics performances steadily improve, the power dissipation of the system components to support them also increases. Power dissipation is generally not an issue when the notebook computer is connected to an external power source such as an AC outlet because the power supply is infinite. When the notebook computer relies on a battery as its power source, however, power dissipation becomes important because the battery has a finite life span after which it needs to be recharged.

It can be inconvenient and annoying for a user to run out of battery charge while he is using his notebook computer, especially if he has no immediate means to recharge the battery. Therefore, maximizing the battery's life span is always desirable to provide the user with at least a

reasonable amount of time to use his notebook computer in a remote place such as on an airplane.

One solution to maximize battery life is offered by the Geyserville™ processor technology developed by the Intel Corporation located in Santa Clara, California. Geyserville extends the battery life by providing a dynamically scalable processor performance. Dynamic scaling refers to automatically adjusting the processor's performance state (processor's clock frequency and supply voltage) depending on the power source. Power dissipation of the processor is proportional to its clock frequency and to the square of its supply voltage. By slowing down the processor's clock and reducing the its supply voltage when the portable system is relying on the battery for its power source, the Geyserville technology dramatically reduces the processor's power dissipation.

The Geyserville solution is only a partial one however, and there is a further need to increase battery life span.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like references indicate similar elements and in which:

Figure 1 is a block diagram of a system in which the method according to one embodiment is implemented.

Figure 2 is a flow diagram of the method according to one embodiment.

DETAILED DESCRIPTION

The present invention extends the dynamic scalability of the Geyserville technology beyond the processor. In one embodiment, system buses and other system components are dynamically scaled.

Scalability refers to increasing or decreasing certain attributes of a system's components such as clock frequencies, supply voltages, graphics performances, buffer strengths, and others. Dynamic scalability refers to scalability upon occurrence of a predetermined event, such as a power management event, without user intervention. In the ensuing description, each attribute is described in relation to two performance states (high level and low level) between which scaling is performed. It is contemplated, however, that each attribute can be scaled among multiple performance states.

Fig. 1 is a block diagram of a system 10 in which the method according to one embodiment of the present invention is implemented. In one embodiment, the system 10 is a computer. In other embodiments, system 10 can be a portable computer, a hand-held electronic device, and the like. In one embodiment, the computer 10 includes a System Management Controller (SMC) 12. The SMC 12 controls the transfer of data between the chipsets and the peripheral devices such as the processor 16, the Input Output Control Hub (I/O CH) 30, the Graphics Memory Control Hub (GMCH) 26, the keyboard 34, and the Input Output Device (I/O Device) 36.

In one embodiment, the SMC 12 is formed of one or more layers including, for example, software, firmware, and hardware. In one embodiment, the SMC 12 is connected to the chipsets and the peripheral devices by a first bus 14. In one embodiment, the first bus is referred to as the System Management Bus (SMBUS). In one embodiment, the chipsets include the GMCH 26 and the I/O CH 30. In one embodiment, the chipsets

provide the electronic interfaces between the processor 16, the memory sub system 20, and the graphics sub system 42.

A bus is a collection of wires through which data is transferred from one part of a computer to another. Two characteristics of every bus are its width and its clock speed. The width determines how much data can be transmitted at one time. For example, a 16-bit bus can transfer 16 bits of data, whereas a 32-bit bus can transmit 32 bits of data. The clock speed is measured in megahertz (MHZ) and indicates how fast the data is transferred. A higher bus clock speed requires a higher minimum bus supply voltage. If the data transmission load on the SMBUS 14 is low, for example, because of low activity, lowering the clock speed and the supply voltage of the SMBUS 14 can reduce the power dissipation of the SMBUS 14.

As stated previously, reducing the power dissipation is generally not an issue when the computer 10 is connected to an external power source such as an AC outlet because the power supply is infinite. When the computer 10 is connected to a battery, however, reducing the power dissipation provides a benefit in the form of increased battery longevity.

In one embodiment, the computer 10 includes an additional bus such as the Memory Bus (MBUS) 34. In one embodiment, the MBUS 34 connects the memory sub system 20 to the GMCH 26. In one embodiment, the MBUS 34 operates at a higher speed than the SMBUS 14.

Fig. 2 is a flow diagram of the method according to one embodiment to be implemented in the computer 10 of Fig. 1.

In one embodiment, the SMC 12 detects the predetermined power management event (at 102). In one embodiment, the power management event includes a change in the power source of the computer 10 from an external source to a battery or vice versa. Upon detecting the power management event, the SMC 12 automatically places the computer in a Low Activity State (at 104). In one embodiment, the Low Activity State includes

the Deep Sleep Power Management State (ACPI Specification C3 State). ACPI Specification stands for Advanced Configuration and Power Interface Specification, Revision 2.0, published on July 27, 2000. During the C3 State, the clock generator 18 input to the components is disabled. That stops all logical functions processing inside the components but allows the internal settings to be maintained (e.g., values stored in registers and caches).

Following, the SMC 12 utilizes a management command structure and an algorithm to send multiplexed commands by utilizing the SMBUS 14 to perform various scaling operations (at 106, 108, 110 and 112). Sending multiplexed commands refers to combining the command signals into one signal for transmission to the multiple components. Two communications devices are used for multiplexing: a multiplexor residing in the SMC 12 to combine the command signals into one signal and a demultiplexor residing in the component unit to separate the command signal pertaining to that component. Sending commands in a multiplexed fashion allows for the scaling operations (at 106-112) to occur simultaneously. In an alternative embodiment, the SMC 12 sends individual commands instead of multiplexed commands.

In one embodiment, performing a scaling operation includes changing the setting of a performance register inside the component. The algorithm contains the predetermined performance register settings and is automatically executed by the SMC 12 upon the occurrence of the power management event. In one embodiment, the algorithm has two predetermined settings (high level and low level) for each of the attributes to be scaled. In other embodiments, programmable devices such as fuse banks and non-volatile memory are used instead of the performance registers.

In one embodiment, the frequencies of the processor clock, the memory sub system clock, and the clock generator 18 are scaled between a high level and a low level (at 106) depending on the power management

event. In one embodiment, the high level is 133 MHZ and the low level is 100 MHZ. The clock frequencies are set to the low level if the computer 10 power source was changed from the outside source to the battery. The clock speeds are set to the high level if the computer 10 power source was changed from the battery to the outside source.

In one embodiment, the setting of the performance register represents bus fraction data specifying the ratio of the component's clock frequency to the clock generator 18 output.

In one embodiment, the buffer strength of the chipset 40 is scaled between a high level and a low level (at 108). The chipset buffers drive the SMBUS 14 and the MBUS 34 by reading data from and writing data onto the buses 14 and 34. The chipset buffers act as holding areas, enabling the processor 16 to manipulate data before transferring it to the buses 14 and 34. The chipset buffers compensate for the speed differences between the processor 16 and the buses 14 and 34. Buffer strength can be scaled between a high level and a low level, based on the data tranmission load and clock frequencies of the buses 14 and 34. A higher buffer strength requires a higher minimum bus supply voltage. By scaling the buffer strength to the low level when the computer 10 is using the battery as its power source, power dissipation is reduced. In one embodiment, the buses speeds are scaled (at 110) between a high level and a low level. In one embodiment, the high level is 133 MHZ and the low level is 100 MHZ. In another embodiment, the high level is 450 MHZ and the low level is 350 MHZ. The bus speeds of the SMBUS 14 and the MBUS 34 are scaled by scaling their respective clock frequencies.

A minimum level of supply voltage is required to support the components clock frequencies and buffer strengths. In the embodiment, depending on the clock frequencies and buffer strengths, supply voltages of the respective components are scaled between a high level and a low level

(at 112). In one embodiment, the high level is 1.8 VDC and the low level is 1.3 VDC.

In another embodiment, the high level is 14.0 VDC and the low level is 8.0 VDC.

In one embodiment, the graphics performances are scaled between a high level and a low level. The high level includes the 4X performance level under the Accelerated Graphics Port (AGP) Interface Specification developed by the Intel Corporation. The low level includes the 2X performance level under the AGP Specification. The 4X performance level requires higher minimum bus speeds and supply voltages than the 2X performance level. It is contemplated that in another embodiment, the low level includes the AGP Specification level 1X.

The present invention thus extends the scalability feature of Geyserville beyond the processor to various components across the computer 10 platform. By scaling to low levels various attributes of the components when a battery power source is utilized, power dissipation of the computer 10 is significantly reduced.

The SMC 12 next determines if all scaling operations have been successfully performed (at 114). In one embodiment, predefined registers including the model-specific registers (MSRs) or component ID registers are read to make that determination. The predefined registers may be updated by the components after the scaling operations have been successfully performed. If the scaling operations were successful, the SMC 12 removes the computer 10 from the Low Activity State (at 116).

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set

forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

In addition, the methods as described above can be stored in memory of a computer system as a set of instructions to be executed. In addition, the instructions to perform the methods as described above could alternatively be stored on other forms of computer-readable mediums, including magnetic and optical disks. For example, the method of the present invention can be stored on computer-readable mediums, such as magnetic disks or optical disks that are accessible via a disk drive (or computer-readable medium drive).

CLAIMS

What is claimed is:

1. A method including:

detecting a power management event in a system; and

dynamically adjusting, in response to the power management event, the performance states of a plurality of system components including system buses.

2. The method of claim 1, wherein the power management event includes a change in the system power source from an AC outlet to a battery or vice versa.

3. The method of claim 1, wherein the system chipset drives the system buses.

4. The method of claim 1, wherein adjusting the performance states of the system buses includes adjusting the chipset buffer strength, the system buses supply voltages and the system buses clock frequencies.

5. The method of claim 1, wherein the components include the memory subsystem, the graphics subsystem and the processor.

6. The method of claim 1, wherein the performance states are adjusted between a high level and a low level.

7. The method of claim 1, wherein adjusting the performance states of the components includes adjusting the components supply voltages and clock frequencies.

8. The method of claim 7, wherein adjusting the performance state of the graphics subsystem includes selecting one predetermined level from two predetermined AGP Specification graphics performance levels.

9. The method of claim 1, wherein dynamically adjusting the performance states includes automatically placing the system in the deep sleep state (ACPI Specification C3 State) upon the occurrence of the power management event to adjust the performance states of the system components.

10. A method including:

detecting a power management event in a system; and

automatically placing the system in a low activity state, in response to the power management event,

adjusting the performance states of a plurality of system buses, and adjusting the performance states of a plurality of system components.

11. The method of claim 10, wherein the power management event includes a change in the system power source from an AC outlet to a battery or vice versa.

12. The method of claim 10, wherein the system chipset drives the system buses.

13. The method of claim 10, wherein adjusting the performance states of the system buses includes adjusting the chipset buffer strength, the system buses supply voltages and the system buses clock frequencies.

14. The method of claim 10, wherein the components include the

processor, the memory subsystem and the graphics subsystem.

15. The method of claim 10, wherein the performance states are adjusted between a high level and low level.

16. The method of claim 10, wherein adjusting the performance state of the components includes adjusting the components supply voltages and clock frequencies.

17. The methods of claim 16, wherein adjusting the performance state of the graphics subsystem includes selecting one predetermined level from two predetermined AGP Specification graphics performance levels.

18. The method of claim 15, wherein the low activity state is the deep sleep state (ACPI Specification C3 State).

19. A system comprising:

a detector adapted to detect generation of a power management event; and

a controller to automatically adjust, in response to the power management event, the performance states of a plurality of system components including system buses.

20. The system of claim 19, wherein the power of management event includes a change in the system power source from an AC outlet to a battery or vice versa.

21. The system of claim 19, wherein the system chipset drives the system buses.

22. The system of claim 19, wherein adjusting the performance states of the system buses includes adjusting the chipset buffer strength, the system buses supply voltages and the system buses clock frequencies.

23. The system of claim 19, wherein the components include the processor, the memory subsystem and the graphics subsystem.

24. The system of claim 19, wherein the performance states are adjusted between a high level and a low level.

25. The system of claim 19, wherein adjusting the performance states of the components includes adjusting the components supply voltages and clock frequencies.

26. The system of claim 25, wherein adjusting the performance state of the graphics subsystem includes selecting one predetermined level from two predetermined AGP Specification graphics performance levels.

27. The system of claim 19, wherein the low activity state is the deep sleep state (ACPI Specification C3 State).

28. An apparatus comprising:

a detector adapted to detect generation of power management event; and

a controller to automatically adjust, in response to the power management event, the performance states of a plurality of system components including system buses.

29. The apparatus of claim 28, wherein the power of management

event includes a change in the system power source from an AC outlet to a battery or vice versa.

30. The apparatus of claim 28, wherein the system chipset drives the system buses.

31. The apparatus of claim 28, wherein adjusting the performance states of the system buses includes adjusting the chipset buffer strength, the system buses supply voltages and the system buses clock frequencies.

32. The apparatus of claim 28, wherein the components include the processor, the memory subsystem and the graphics subsystem.

33. The apparatus of claim 28, wherein the performance states are adjusted between a high level and a low level.

34. The apparatus of claim 28, wherein adjusting the performance states of the components includes adjusting the components supply voltages and clock frequencies.

35. The apparatus of claim 34, wherein adjusting the performance state of the graphics subsystem includes selecting one predetermined level from two predetermined AGP Specification graphics performance levels.

36. The apparatus of claim 28, wherein the low activity state is the deep sleep state (ACPI Specification C3 State).

37. A computer-readable medium having stored thereon a set of instructions to translate instructions, the set instructions, which when

executed by a processor, cause the processor to perform a method comprising:

detecting a power management event in a system; and

dynamically adjusting, in response to the power management event, the performance states of a plurality of system components including system buses.

38. The computer-readable medium of claim 37, wherein the power management event includes a change in the system power source from an AC outlet to a battery or vice versa.

39. The computer-readable medium of claim 37, wherein the chipset drives the system buses.

40. The computer-readable medium of claim 37, wherein adjusting the performance states of the system buses includes adjusting the chipset buffer strength, the system buses supply voltages and the system buses clock frequencies.

41. The computer-readable medium of claim 37, wherein the components include the memory subsystem, the graphics subsystem and the processor.

42. The computer-readable medium of claim 37, wherein the performance states are adjusted between a high level and a low level.

43. The computer-readable medium of claim 37, wherein adjusting the performance states of the components includes adjusting the components supply voltages and clock frequencies.

44. The computer-readable medium of claim 43, wherein adjusting the performance state of the graphics subsystem includes selecting one predetermined level from two predetermined AGP Specification graphics performance levels.

45. The computer-readable medium of claim 37, wherein dynamically adjusting the performance states includes automatically placing the system in the deep sleep state (ACPI Specification C3 State) upon the occurrence of the power management event to adjust the performance states of the system components.

ABSTRACT OF THE DISCLOSURE

A method and apparatus to detect a power change in a system (e.g. computer) and to automatically adjust, in response to the power change, the performance states (e.g. supply voltages, clock frequencies and buffer strengths) of a plurality of system components (e.g. buses). The apparatus includes a detector and a controller.

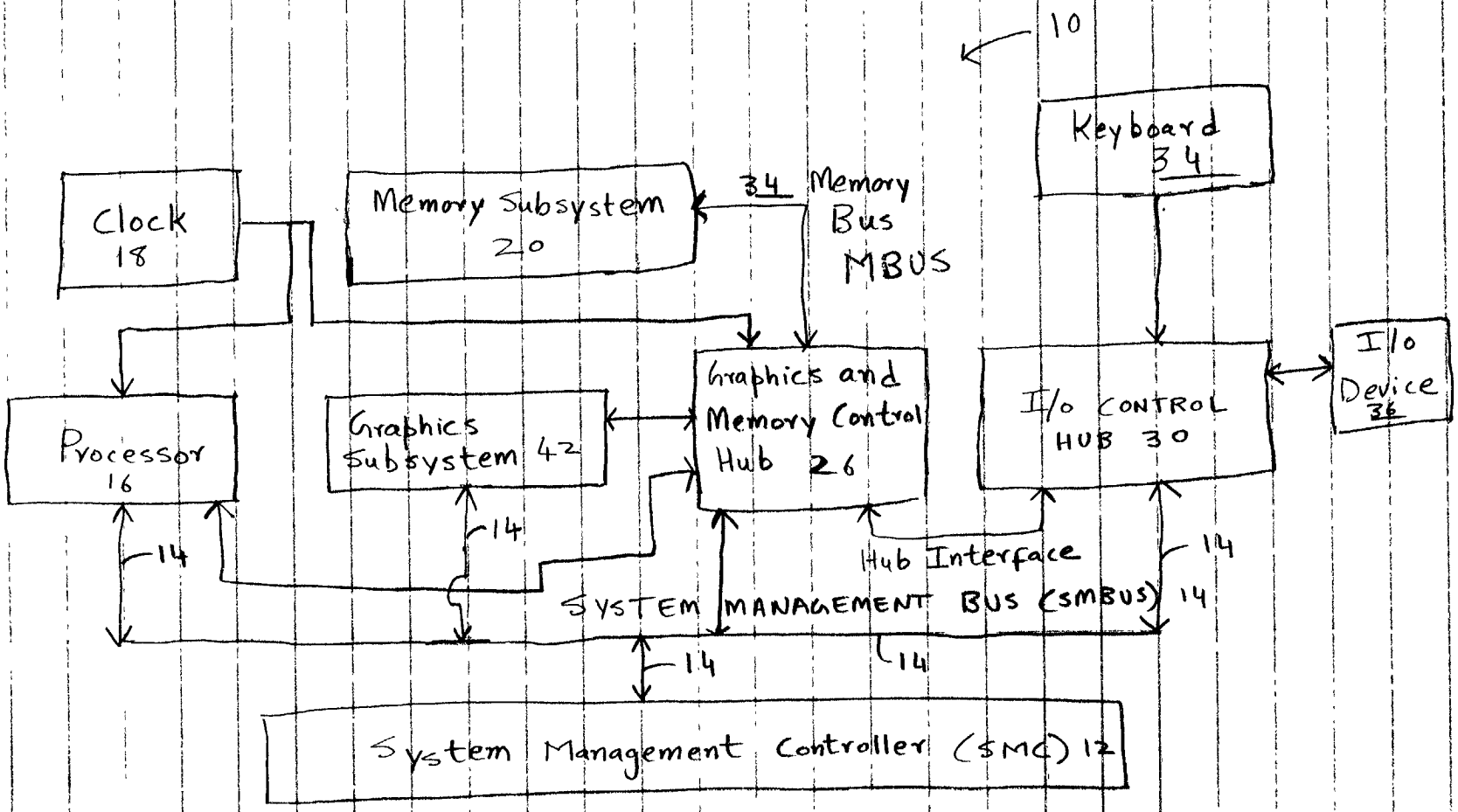

Fig. 1

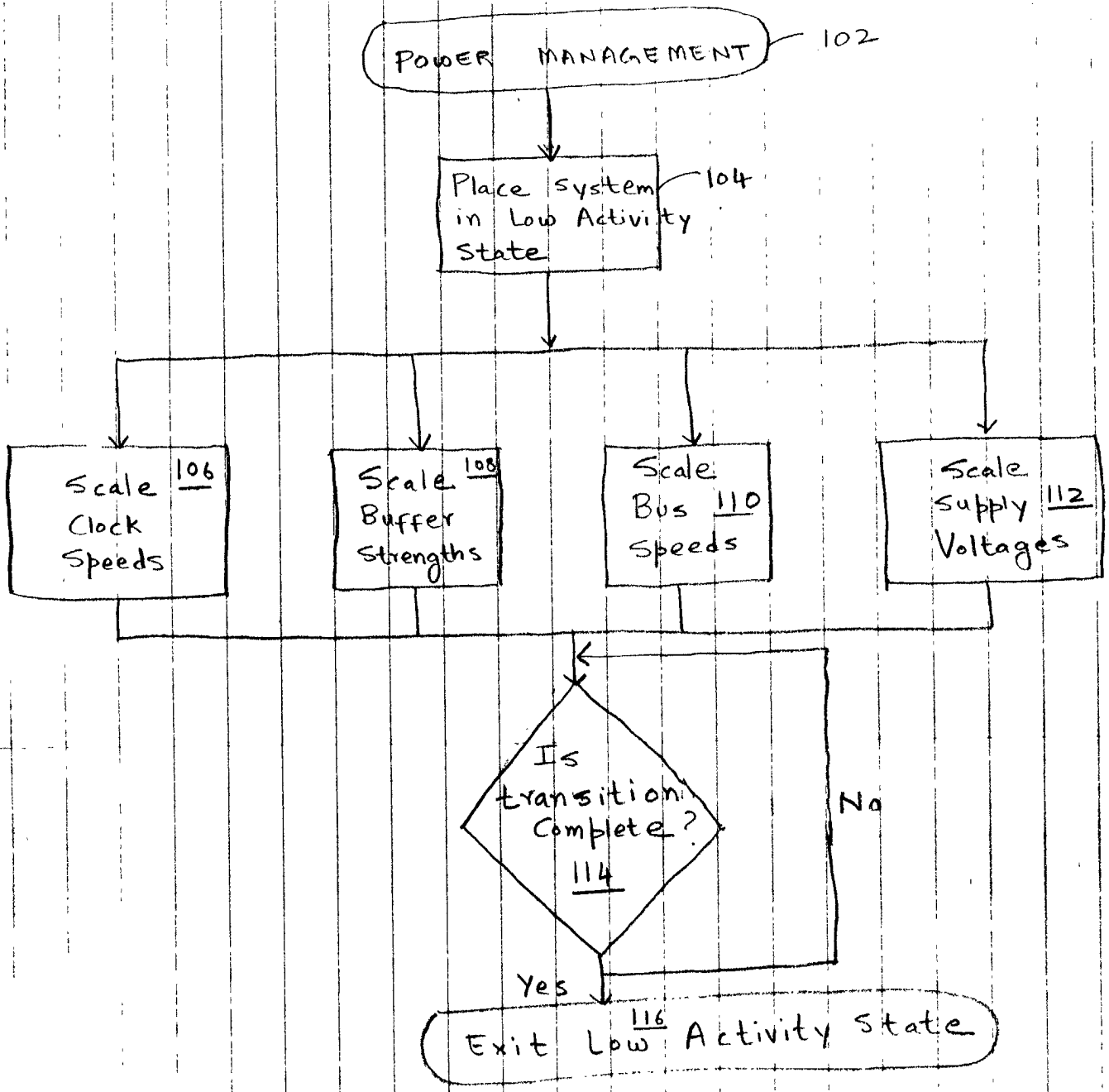

Fig. 2

Attorney's Docket No.: 042390.P9737 Patent

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
METHOD AND APPARATUS FOR PROVIDING DYNAMICAL SCALABILITY

the specification of which

_X_ is attached hereto.
___ was filed on (MM/DD/YYYY) _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on (MM/DD/YYYY) _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Foreign Filing Date - MM/DD/YYYY)	Yes	No
(Number)	(Country)	(Foreign Filing Date - MM/DD/YYYY)	Yes	No
(Number)	(Country)	(Foreign Filing Date - MM/DD/YYYY)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

(Application Number)	(Filing Date – MM/DD/YYYY)
(Application Number)	(Filing Date – MM/DD/YYYY)

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number)	(Filing Date – MM/DD/YYYY)	(Status -- patented, pending, abandoned)
(Application Number)	(Filing Date – MM/DD/YYYY)	(Status -- patented, pending, abandoned)

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to John P. Ward (Name of Attorney or Agent), BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct telephone calls to John P. Ward (Name of Attorney or Agent), (408) 720-8300.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor Tony Hamilton

Inventor's Signature ______________________ Date ______________

Residence ______________________ Citizenship ______________
(City, State) (Country)

Post Office Address ______________________

APPENDIX A

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APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.